REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline 3. Change conditions for Supply Current test I_{EE}. Editorial changes throught.	92-01-17	M. A. Frye
B	Update to current requirements. Editorial changes throughout. – drw	02-02-25	Raymond Monnin

THE FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
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REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Joseph A. Kerby

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles E. Besore

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-08-30

MICROCIRCUIT, LINEAR, 12-BIT VOLTAGE OUTPUT D/A CONVERTER, MICROPROCESSOR COMPATIBLE, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
B	A	**67268**	**5962-88659**

SHEET 1 OF 12

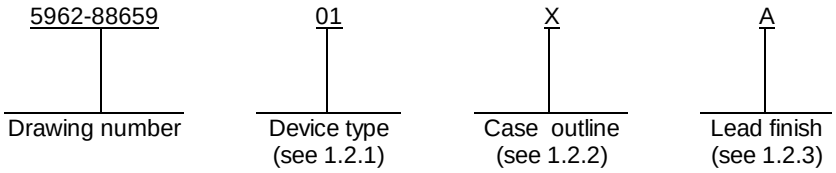
DSCC FORM 2233
APR 97

5962-E228-02

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD667	D/A converter, 12-bit, voltage output, microprocessor compatible

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line
3	CQCC1-N28	28	square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{CC} to power ground range	0 V dc to +18 V dc
V_{EE} to power ground range	0 V dc to -18 V dc
Digital inputs (pins 11-15, 17-28) to power ground range	-1.0 V dc to 7.0 V dc
Reference in to reference ground	±12 V dc
Bipolar offset to reference ground	±12 V dc
10 V span R to reference ground	±12 V dc
20 V span R to reference ground	±24 V dc
Reference out, V_{OUT} (pins 6 and 9)	continuous short to power ground, momentary short to V_{CC}
Power dissipation (P_D)	1,000 mW 1/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case outline X	60°C/W
Case outline 3	125°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+11.4 V dc to +16.5 V dc
Supply voltage range (V_{EE})	-11.4 V dc to -16.5 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Truth table. The truth table shall be as specified on figure 3.

3.2.5 Timing diagram. The timing diagram shall be as specified on figure 4.

3.2.6 Test circuit for 20 V FSR. The test circuit for 20 V FSR shall be as specified on figure 5.

3.2.7 Test circuit for 10 V FSR. The test circuit for 10 V FSR shall be as specified on figure 6.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Resolution	RES				All	12		Bits
Integral linearity error	LE	2/		1	All	-0.5	+0.5	LSB
				2, 3		-0.75	+0.75	
Differential linearity error	DLE	2/		1	All	-0.75	+0.75	LSB
				2, 3		-1	+1	
Gain error	A_E	All bits high		1	All	-0.2	+0.2	% of FSR
Gain drift 4/	$\Delta A_E/\Delta T$			2, 3		-30	+30	ppm of FSR/°C
Unipolar offset error	V_{OS}	All bits low		1	All	-2	+2	LSB
Unipolar offset drift 4/	$\Delta V_{OS}/\Delta T$			2, 3		-3	+3	ppm of FSR/°C
Bipolar zero error 5/	B_{PZE}	MSB high, all other bits low		1	All	-0.1	+0.1	% of FSR
Bipolar zero drift 4/, 5/	$\Delta B_{PZE}/\Delta T$			2, 3		-10	+10	ppm of FSR/°C
Reference voltage	V_{REF}	V_{CC} = +11.4 V, V_{EE} = -11.4 V 6/		1, 2, 3	All	9.9	10.1	V
Latch functionality	$V_{OS\Delta}$	7/		1, 2, 3	All	-1	+1	LSB
	$A_{E\Delta}$	7/, 8/				-1	+1	
Output current	I_{OUT}	T_A = +25°C 9/		1	All	-5	+5	mA
Output short circuit current	I_{OS}	T_A = +25°C 9/		1	All		40	mA
Power supply rejection ratio	PSSR+	+11.4V ≤ V_{CC} ≤ +16.5 V, All bits high, T_A = +25°C		1	All	-10	+10	ppm of FS/%
	PSSR-	-16.5V ≤ V_{EE} ≤ -11.4 V, All bits high, T_A = +25°C				-10	+10	
Power supply current	I_{CC}	V_{CC} = +16.5 V, V_{EE} = -16.5 V T_A = +25°C	All bits high	1	All		12	mA
	I_{EE}		All bits low			-25		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital input high voltage	V_{IH}	T_A = +25°C	1	All	2.0		V
Digital input low voltage	V_{IL}		1	All		0.8	V
			2, 3			0.7	
Digital input high current	I_{IH}	T_A = +25°C, V_{IH} = 5.5 V	1	All		10	µA
Digital input low current	I_{IL}	T_A = +25°C, V_{IL} = 0 V	1	All		5	µA
Functional tests		See 4.3.1c	7, 8	All			
Output voltage settling time	t_{SL}	R_L = 2 kΩ, 9/ C_L = 500 pF, See figure 5 20 V FSR	9	All		4	µs
		T_A = +25°C, See figure 4, See figure 6 10 V FSR				3	
$\overline{CS}$ pulse width	t_{CP}	T_A = +25°C, See figure 4, 9/	9	All	100		ns
Data setup time	t_{DC}	T_A = +25°C, See figure 4, 9/	9	All	50		ns
Data hold time	t_{DH}	T_A = +25°C, See figure 4, 9/	9	All	0		ns
Address valid to end of $\overline{CS}$	t_{AC}	T_A = +25°C, See figure 4, 9/	9	All	100		ns

1/ V_{CC} = +15 V dc, V_{EE} = -15 V dc, $\overline{CS}$, A0, A1, A2, A3 = logic "0", V_{IH} =2.0 V, V_{IL} = 0.8 V, 50Ω resistor pin 6 to pin 7. Unipolar configuration (pins 1 and 2 to pin 9, pin 4 to pin 5, unless otherwise specified).

2/ All bits with positive errors on. All bits with negative errors on.

3/ Major carry transitions.

4/ $\Delta V_{OS}/\Delta t$, $\Delta A_E/\Delta t$, $\Delta B_{PZE}/\Delta t$ are determined for measurements made at +125°C, +25°C, and -55°C for V_{OS}, A_E, and B_{PZE} respectively. Drift is specified from +25°C to +125°C and from +25°C to -55°C.

5/ Bipolar configuration (pins 1 to 9, 50Ω resistor pin 4 to pin 6).

6/ In subgroup 1, the reference output is loaded with 0.5 mA nominal reference current, 1.0 mA bipolar offset current and 0.1 mA additional current. In subgroups 2 and 3, only the 0.5 mA reference input current is applied. The reference must be buffered to supply external loads at elevated temperatures.

7/ All bits low, A0, A1, A2, A3 are logic "0"; A0, A1, A2, A3 are initialized to logic "1", each 4-bit register set to logic "1", and A0, A1, A2 are set sequentially to logic "0" and back to logic "1" to latch data into first rank.

8/ A3 is set to logic "0" and back to logic "1" to latch full scale output into second rank.

9/ Guaranteed, if not tested, to the limits specified.

Device type	01
Case outline	X and 3
Terminal number	Terminal symbol
1	20 V SPAN
2	10 V span
3	SUM JCT
4	BIP OFF
5	AGND
6	V_{REF} OUT
7	V_{REF} IN
8	V_{CC}
9	V_{OUT}
10	V_{EE}
11	$\overline{CS}$
12	A3
13	A2
14	A1
15	A0
16	POWER GND
17	DB0 (LSB)
18	DB1
19	DB2
20	DB3
21	DB4
22	DB5
23	DB6
24	DB7
25	DB8
26	DB9
27	DB10
28	DB11 (MSB)

FIGURE 1. Terminal connections.

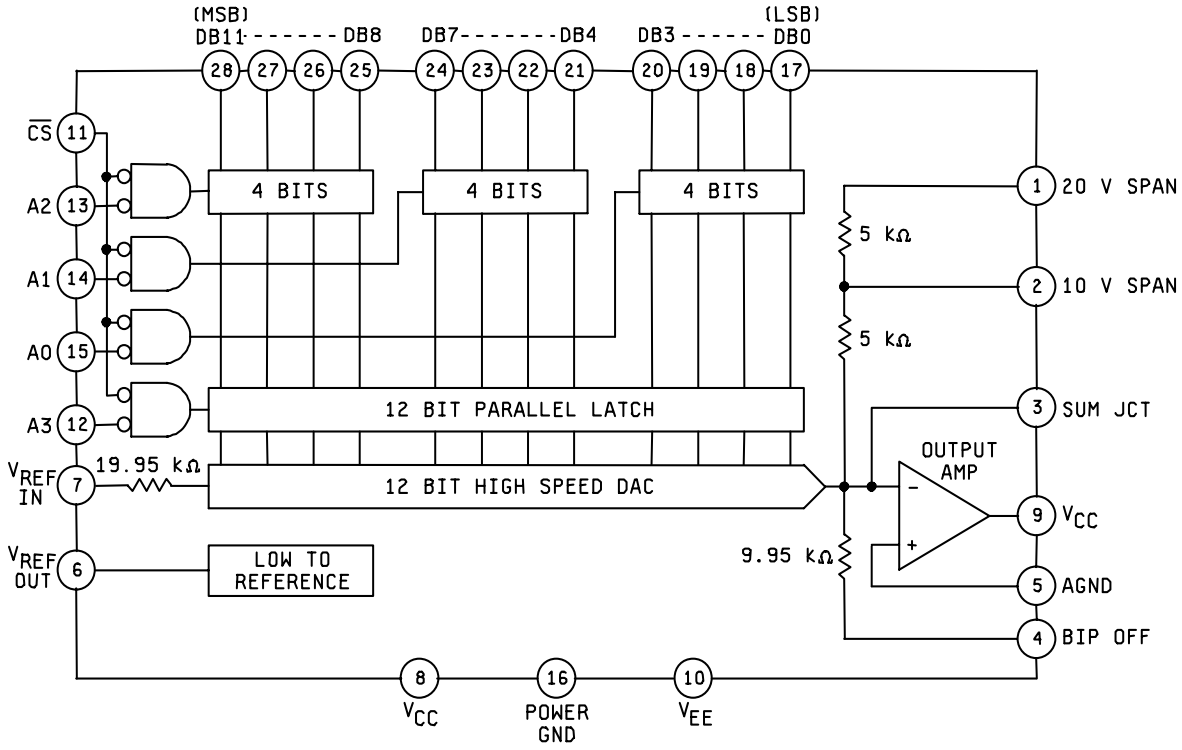


FIGURE 2. Block diagram.

$\overline{CS}$	A3	A2	A1	A0	Operation
1	X	X	X	X	No operation
X	1	1	1	1	No operation
0	1	1	1	0	Enable 4 LSBs of first rank
0	1	1	0	1	Enable 4 middle bits of first rank
0	1	0	1	1	Enable 4 MSBs of first rank
0	0	1	1	1	Loads second rank from first rank
0	0	0	0	0	All latches transparent

"X" = Don't care.

FIGURE 3. Truth table.

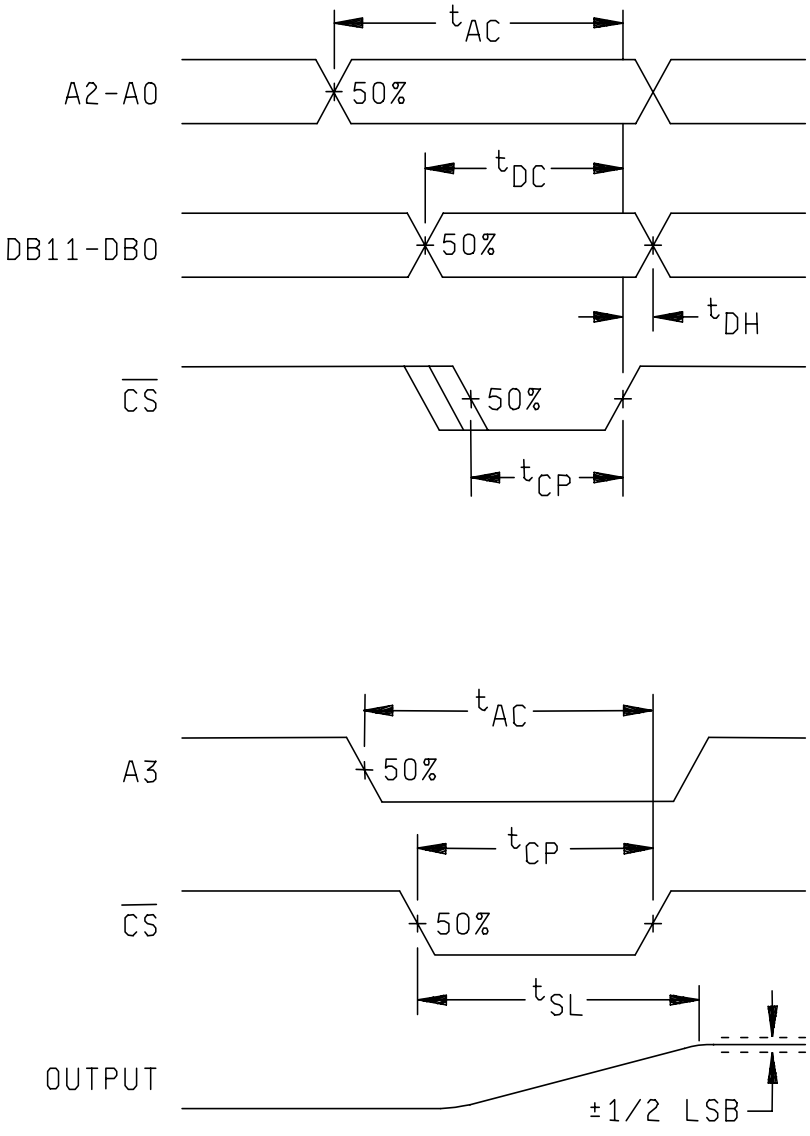
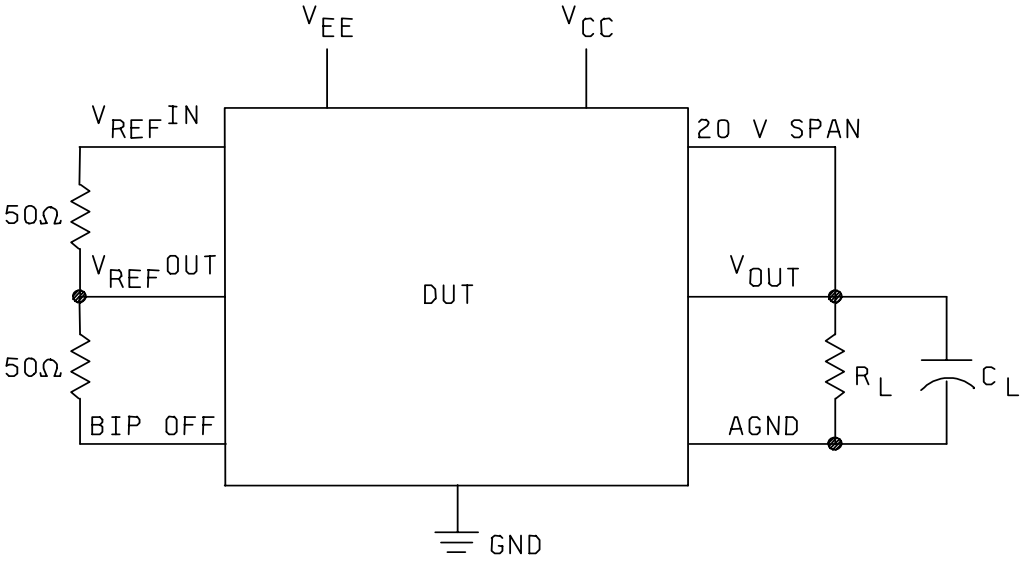
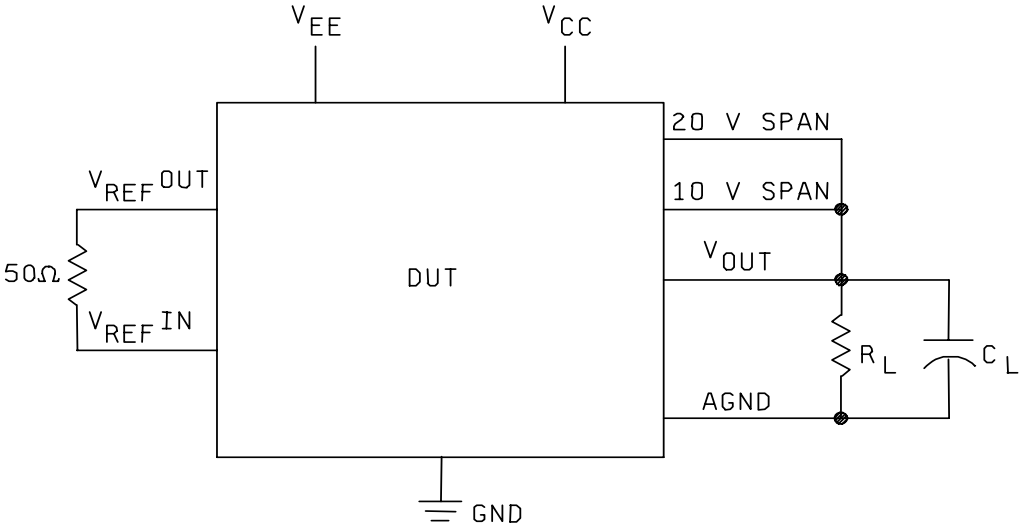


FIGURE 4. Timing waveforms.



NOTE: ±10 V bipolar voltage output.

FIGURE 5. Test circuit for 20 V FSR.



NOTE: 0 V to +10 V unipolar voltage output.

FIGURE 6. Test circuit for 10 V FSR.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroup 9, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-02-25

Approved sources of supply for SMD 5962-88659 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-88659013A	24355	AD667SE/883B
5962-8865901XA	24355	AD667SD/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462